MonolithIC 3D Inc.

SEMICONDUCTOR IP CASE STUDY

How a sixteen-year fabless semiconductor company turned a monolithic 3D integration thesis into 406 issued US patents and licensing revenues.

INTRODUCTION

MonolithIC 3D Inc. builds the foundational intellectual property for stacking semiconductor devices vertically rather than shrinking them horizontally. Founded in 2009 by Zvi Or-Bach in Silicon Valley and Isreal, the company set out from a single premise: that transistor cost scaling would stall, and that the industry would have to move into the third dimension to keep improving performance per watt and per dollar. At the time this was a minority view. Google confirmed it publicly at IEDM 2023, reporting that transistor cost scaling stalled at 28 nm and has stayed flat generation over generation.

As a fabless semiconductor play, the company chose to express that thesis almost entirely as patents. It does not fabricate chips. Its product is a claim set, and the value of that product depends on how carefully and how continuously the filings were made. That makes the prosecution programme itself the business, and it is the reason the portfolio now supports licensing and enforcement rather than sitting on a shelf.

BACKGROUND

The first two patents, US 7,960,242 and US 7,964,916, issued in June 2011 on applications carrying 2009 and 2010 priority. The company has produced issued patents in every calendar year since. As of the July 14, 2026 grant of US 12,684,778, the published list runs to 406 unique issued US patents, with the company's Record of Invention placing pending applications above 350. The estate is a memory portfolio with a logic and packaging perimeter. Across the published titles, 106 name memory, 49 name metal layers, 24 name bonding, 13 name logic, 10 name transistors and 10 name image sensors. Individual filings anticipated techniques the industry adopted years later: the SiGe cut layer of WO 2017/053329 and US 10,515,981, and power delivery from below the device layer in US 8,395,191, drawn from a 2009 priority filing and now the industry-standard backside power approach.

That continuity converted into commercial results. In mid-2025 the world's largest memory maker took a licence to the portfolio. The International Trade Commission has since instituted two Section 337 investigations on the portfolio: No. 337-TA-1492, instituted March 26, 2026 on eight patents with a target completion date of August 30, 2027, and No. 337-TA-1506, instituted June 10, 2026 on five more. Several of the asserted patents issued only months before they were asserted, which is only possible when the filing cadence never slowed.

The independent validation followed the same curve. Alibaba's ISSCC 2022 result on a monolithic 3D architecture reported a 9.78x speedup, 317x better energy efficiency and 660x better area efficiency against a 14 nm Xeon baseline using 55 nm logic. AMD shipped 3D V-Cache. Kioxia and SanDisk began sampling BiCS10 at 332 layers in July 2026 and SK hynix reached 321 layers. In November 2025 the company took the Best Paper Award at IEEE TENCON for charge trap-based 3D DRAM. A thesis filed in 2009 is now the roadmap the industry is executing, and the patents were in place before it got there.

> ***"We were developing 3D semiconductor technology and patenting against a thesis the industry did not accept yet. Everything depended on the patent work by PatentPC to protect our work."***
>
> ZVI OR-BACH, CEO MONOLITHIC 3D INC.

LEADERSHIP

ZVI OR-BACH

Founder, President and Chief Executive Officer

Zvi Or-Bach is a three-time semiconductor founder. He earned a BSc in electrical engineering cum laude from the Technion in 1975 and an MSc with distinction in computer science from the Weizmann Institute in 1979. In 1989 he founded Chip Express and ran it as president and CEO for ten years, building it to $40M in revenue before its acquisition. In 1999 he founded eASIC, serving as CEO for six years and raising three successive rounds from Vinod Khosla and Kleiner Perkins; eASIC won the EE Times ACE Award for Ultimate Product of the Year in 2005 and was acquired by Intel in 2018. He has led MonolithIC 3D since 2009 and holds over 460 issued patents in his own name. He chairs the board of Zeno Semiconductors, formerly chaired the 3D track of the IEEE S3S Conference, and has authored four chapters of NANO-CHIPS 2030 and a chapter of Chips 2020 Vol. II.

THE PATENTPC APPROACH

What first set PatentPC apart was the breadth of technology it could take on and the degree to which PatentPC met our needs. A portfolio of this size and cadence is not a series of one-off engagements; it is a manufacturing line for claims, and it has to be run like one. PatentPC handles filings in every United States jurisdiction and require little time from the inventors to set a matter in motion, which matters enormously when one of the inventors is also the chief executive.

The work on a semiconductor structures portfolio is unusually demanding on the drafting side. Claims have to cover a fabrication result without being confined to a single process recipe, because the licensee's process will not be the one described in the specification. They have to be varied deliberately in scope across a family so that the broadest claims can absorb a validity challenge without taking the commercially important ones down with them. And every argument entered in a response becomes part of a public record that a future adversary will read line by line.

We had big law handling our IP, but switched to PatentPC with its fixed fee and responsiveness. On a programme measured in hundreds of filings, that efficiency is what makes a sustained cadence affordable in the first place. PatentPC worked with our in-house patent department and helped us with:

- Claim scope graduated across the family. Broad claims, intermediate claims and narrow product-reading claims are drafted deliberately rather than emerging by accident from prosecution.
- An examiner interview on every office action. No exceptions and no extra charge, both to raise allowance rates and to keep the written estoppel record as short as possible.
- Drafting to the fabrication result, not the recipe. Structure claims are written to read on a device as built, independent of the specific process flow used to build it.
- Dual docketing. Every date is docketed twice, by two people, in two systems, and reconciled weekly.
- Fixed fees agreed before work begins, on applications, continuations and office-action responses alike, so our IP programme can be budgeted rather than estimated.

RESULTS

688+
ISSUED US PATENTS

660
INTERNATIONAL PATENTS

350+
APPLICATIONS PENDING

The portfolio grew from five issued patents in 2011 to a peak of 59 grants in 2021, followed by 53 in 2022, 44 in 2023 and 50 in 2024. Sixteen consecutive years of issuance, with no gap and no severed chain, is the outcome that matters most: it means the 2009 and 2010 priority dates are still live in filings being made today.

Patent families: 335
Granted patents: 688
Applications: 317
U.S. filings: 371

International (WO) filings: 660 ← your answer
Europe (EP): 10
China (CN): 9
Rest of world: 3

> ***"We at MonolithIC 3D been working with Bao Tran over many years. Mr. Tran was always available to help us with any patents related issue. Mr. Tran is always bee very knowledgeable and efficient and we been very happy to have him as part of our team. We highly recommend him."*** ZVI OR-BACH, CEO, MONOLITHIC 3D INC.

Build a portfolio that holds its priority

Whether you are filing your first application or running a continuation programme sixteen years deep, the same two things decide what the estate is worth later: how the claims are drafted, and whether the chain ever breaks. PatentPC can map every live continuation chain in your portfolio and show you where the exposure is, at no charge and before you move any work. Talk to us about what you are building.

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