TARTAN SILICON

SEMICONDUCTOR IP CASE STUDY

How a boutique fabless semiconductor company turned one founder's invention into a defensible asset with PatentPC

INTRODUCTION

Tartan Silicon Systems, Inc. delivers value through expertise in product engineering, semiconductor operations, and data science. Through that expertise, its processes, and its patented manufacturing analytics technology, Tartan enables customers to reach optimal profitability with highly reliable products — working across the full product lifecycle, from design through production.

Tartan's analytics improve product traceability, quality, yield, and reliability, helping customers build highly reliable systems-on-chip for the long term. Its offering spans new product introduction services, device traceability from fab to field, and patented field-failure prediction technology that lets a device self-identify as likely to fail so preventative maintenance can happen before the system goes down. The priority markets are automotive, aerospace and defense, and high-performance computing — the places where a single field failure is catastrophically expensive.

BACKGROUND

Founded in Napa, California in 2016 with the mission of eliminating field failures of electronic systems, Tartan began as a services and analytics business. Its reputation was built on delivery: partnering with Synergie-CAD on chip productization projects, enabling Imagination Technologies to ship high-quality WiFi transceivers to global customers, and providing Infinera the manufacturing analytics needed to hit chip volume, quality, and reliability goals.

Then the technology evolved past services. Tartan developed a set of on-chip monitoring sensors read during wafer probe, final test, and field operation, feeding a machine learning model trained on sample devices stressed in the lab until failure. The output is a failure prediction model for silicon in the field. That is no longer a consulting methodology — it is an invention, and in a $1 trillion industry it is exactly the kind of invention that large IDMs, EDA vendors, and test houses build internally the moment they see it work.

Tartan faced the classic boutique dilemma. A small, expert-heavy company competing against enormous incumbents cannot out-file them, and cannot fund a sprawling portfolio. It needed one thing done extremely well: a single foundational application, drafted broadly enough to cover the sensor-plus-stress-generator-plus-machine-learning architecture as a system, and prosecuted to issuance before the technology was presented at IEEE webinars, SEMICON West, and customer engagements. Enter PatentPC.

> ***"In this industry the technology is the company. If the on-chip monitoring and prediction architecture were not protected before we started showing it, we would have handed our differentiation to companies a thousand times our size."***
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> ALAN ARONOFF, FOUNDER & CEO, TARTAN SILICON SYSTEMS, INC.

LEADERSHIP

ALAN ARONOFF

Founder, President & CEO, Tartan Silicon Systems, Inc.

Alan Aronoff founded Tartan in October 2016 after four decades in the semiconductor industry — VP and General Manager at Synopsys, General Manager at NEC Electronics, Director of Engineering at Mostek, SVP of Marketing and Business Development at Key ASIC, VP of Operations and IP Licensing at Anchor Bay Technologies, and Strategic Development at Imagination Technologies. He holds a BS in electrical and biomedical engineering from Carnegie Mellon and an MS in electrical engineering from Southern Methodist University.

SOLUTION

PatentPC serves us well because it operates like a strategic extension of the executive team—combining patent prosecution, competitive intelligence, and commercialization strategy into one integrated engine. Instead of treating patents as isolated legal filings, PatentPC maps each invention to market trajectories, competitor behavior, and long-term defensibility. Our company benefits from this because PatentPC reduces wasted R&D spend, strengthens negotiation leverage, and ensures every filing supports a broader business objective. The firm's AI-enhanced workflows accelerate drafting, prior-art analysis, and claim-shaping, giving corporate teams faster cycles and higher-quality filings without sacrificing legal rigor.

Equally important, PatentPC is built for operational reliability at scale. We get predictable processes, deadline-proof systems, and a team that understands how to navigate USPTO complexities, international filings, and portfolio management with precision. The firm's emphasis on founder psychology and clear communication also translates well to corporate environments—turning complex patent strategy into actionable, executive-ready insights. The result is a partner that not only protects innovation but amplifies it, helping corporations move faster, reduce risk, and build durable competitive moats. They worked with us on:

- System-level claiming — sensors, on-die stress generator, and data interface claimed as an integrated circuit rather than as a software method, keeping the claim firmly on the hardware side of Section 101.
- Lifecycle coverage — claim language reaching data captured during wafer manufacturing and during operation, so the protection follows the device from fab to field.

- Filing ahead of disclosure — on file before conference talks, webinars, and customer demonstrations put the architecture in public view.
- Domain-fluent counsel — attorneys already conversant in wafer test, aging, and reliability analytics, so no education bill.
- Boutique economics — depth and prosecution quality of a large-firm filing at a cost a founder-funded company can carry.

RESULTS

2	2025-2026	3
FOUNDATIONAL US PATENT ISSUED	GRANT DATE	PRIORITY MARKETS COVERED

US Patent 12,203,973, “Monitoring semiconductor reliability and predicting device failure during device life” covers a circuit with one or more sensors formed on one or more dies detecting wafer characterization data, an on-die stress generator that places those sensors under stress during wafer manufacturing or operation, and an interface communicating the data to a processor or tester — the architecture, not just an algorithm.

That single asset does disproportionate work. Tartan can now describe its technology as patented in customer conversations, marketing materials, and conference presentations without exposing the differentiation. For automotive and aerospace customers running multi-year qualification cycles, an issued patent is a supply-chain durability signal as much as a legal one. And for a company of Tartan’s size, it converts founder know-how into a balance-sheet asset that survives any single engagement.

By working with experienced attorneys backed by a technology stack, it avoided paying outside counsel to learn reliability physics and wafer test, and received an application with more technical depth on a far shorter cycle. By making the change, Tartan now pays less while receiving more accurate and more efficient patent services — with claim drafting and strategic advice still owned by its patent attorneys.

> ***“PatentPC’s ability to navigate complex chip technology and keeping costs in line for us was exceptional. I participated in the PTO interview session with Attorney Bao Tran and saw how he bridges the differences between the inventor and the examiner. I was thrilled by the resulting patents.”***
>
> ALAN ARONOFF, FOUNDER & CEO, TARTAN SILICON SYSTEMS, INC.

One great patent beats ten weak ones.

PatentPC pairs experienced patent attorneys with practice automation so boutique semiconductor companies can protect their core invention properly — broad claims, fast prosecution, founder-friendly economics. Talk to us about a portfolio strategy for your technology.